IN THE CLAIMS:

1. (Currently amended) A method of deriving an output clock signal from a received data signal comprising the steps of:

(a) coupling a fixed frequency input clock signal to a multitap delay line, having outputs that provide respectively different phase delayed versions of said fixed frequency input clock signal;

(b) coupling one of said outputs of said multitap delay line to an output port from which said output clock signal is derived; and

(c) controllably coupling another of said outputs of said multitap delay line to said output port so as to change said output clock signal in accordance with a ~~relationship~~processed comparison between said received data signal and said output clock signal, in which said processed comparison results from applying the output from an unprocessed comparison to a series of processing elements consisting of an error filter, a gain element and a frequency accumulator.

2. (Original) The method according to claim 1, wherein step (c) comprises controllably coupling to said output port an output of said multitap delay line that provides a later-in-time delay relative to said one of said outputs of said multitap delay line, in response to said output clock signal exhibiting a clock frequency that is higher than the frequency of said received data signal, thereby reducing the frequency of said output clock signal.

3. (Original) The method according to claim 1, wherein step (c) comprises controllably coupling to said output port an output of said multitap delay line that provides an earlier-in-time delay relative to said one of said outputs of said multitap delay line, in response to said output clock signal exhibiting a clock frequency that is lower than the frequency of said received data signal, thereby increasing the frequency of said output clock signal.

4. (Original) The method according to claim 1, wherein step (c) comprises phase-comparing said received data signal with said output clock signal to derive a phase error signal, and controllably coupling another of said outputs of said multitap delay line to said output port so as to change said output clock signal in accordance with whether said received data signal is advanced or retarded relative to said output clock signal.

5. (Original) The method according to claim 1, wherein step (c) comprises phase-comparing said received data signal with said output clock signal to derive a phase error signal, and periodically, over an interval of plural cycles of said output clock signal, coupling another of said outputs of said multitap delay line to said output port so as to change said output clock signal in accordance with whether said received data signal is advanced or retarded relative to said output clock signal.

6. (Currently amended) An apparatus for deriving an output clock signal from a received data signal comprising:

a multitap delay line, to which a fixed frequency input clock signal is applied, said multitap delay line having a plurality of outputs that provide respectively different phase delayed versions of said fixed frequency input clock signal;

a multiplexer having a plurality of inputs respectively coupled to said plurality of outputs of said multitap delay line, and being controllably operative to couple one of said outputs of said multitap delay line to an output port from which said output clock signal is derived; and

a control circuit, which is operative to selectively change which of said outputs of said multitap delay line is coupled by said multiplexer to said output port, so as to controllably change said output clock signal in accordance with a relationship between said received data signal and said output clock signal, said control circuit consists of a comparison element receiving said received data signal and said output clock signal and providing a comparison output to a series connection of an error filter, a gain element and a frequency accumulator.

7. (Original) The apparatus according to claim 6, wherein said control circuit is operative to cause said multiplexer to controllably couple said output port to an output of said multitap delay line that provides a later-in-time delay relative to said one of said outputs of said multitap delay line, in response to said output clock signal exhibiting a clock frequency that is

higher than the frequency of said received data signal, thereby reducing the frequency of said output clock signal.

8. (Original) The apparatus according to claim 6, wherein said control circuit is operative to cause said multiplexer to controllably couple said output port to an output of said multitap delay line that provides an earlier-in-time delay relative to said one of said outputs of said multitap delay line, in response to said output clock signal exhibiting a clock frequency that is lower than the frequency of said received data signal, thereby increasing the frequency of said output clock signal.

9. (Original) The apparatus according to claim 6, wherein said control circuit is operative to phase-compare said received data signal with said output clock signal to derive a phase error signal, and to cause said multiplexer to controllably couple another of said outputs of said multitap delay line to said output port so as to change said output clock signal in accordance with whether said received data signal is advanced or retarded relative to said output clock signal.

10. (Original) The apparatus according to claim 6, wherein said control circuit is operative to phase-compare said received data signal with said output clock signal to derive a phase error signal, and to periodically cause, over an interval of plural cycles of said output clock signal, said multiplexer to couple another of said outputs of said multitap delay line to said output

port so as to change said output clock signal in accordance with whether said received data signal is advanced or retarded relative to said output clock signal.

11. (Currently Amended) An apparatus for deriving an output clock signal from a received data signal comprising:

a fixed fractional delay line having an input port coupled to receive a fixed frequency input clock signal, said fixed fractional delay line having a plurality of outputs that provide respectively different phase delayed versions of said fixed frequency input clock signal;

a multiplexer having a plurality of inputs respectively coupled to said plurality of outputs of said fixed fractional delay line, and being controllably operative to couple one of said outputs of said fixed fractional delay line to an output port from which said output clock signal is derived; and

a control loop, coupled between the output and a steering control input of said multiplexer circuit, and being operative to selectively change which of said outputs of said fixed fractional delay line is coupled by said multiplexer to said output port, so as to controllably change said output clock signal in accordance with a relationship between said received data signal and said output clock signal, in which said control loop consists of a comparison element receiving said received data signal and said output clock signal and providing a comparison output to a series connection of an error filter, a gain element and a frequency accumulator.

12. (Original) The apparatus according to claim 11, wherein said control loop is operative to cause said multiplexer to controllably couple said output port to an output of said fixed fractional delay line that provides a later-in-time delay relative to said one of said outputs of said fixed fractional delay line, in response to said output clock signal exhibiting a clock frequency that is higher than the frequency of said received data signal, thereby reducing the frequency of said output clock signal.

13. (Original) The apparatus according to claim 11, wherein said control loop is operative to cause said multiplexer to controllably couple said output port to an output of said fixed fractional delay line that provides an earlier-in-time delay relative to said one of said outputs of said fixed fractional delay line, in response to said output clock signal exhibiting a clock frequency that is lower than the frequency of said received data signal, thereby increasing the frequency of said output clock signal.

14. (Original) The apparatus according to claim 11, wherein said control loop is operative to phase-compare said received data signal with said output clock signal to derive a phase error signal, and to cause said multiplexer to controllably couple another of said outputs of said fixed fractional delay line to said output port so as to change said output clock signal in

accordance with whether said received data signal is advanced or retarded relative to said output clock signal.

15. (Original) The apparatus according to claim 11, wherein said control loop is operative to phase-compare said received data signal with said output clock signal to derive a phase error signal, and to periodically cause, over an interval of plural cycles of said output clock signal, said multiplexer to couple another of said outputs of said fixed fractional delay line to said output port so as to change said output clock signal in accordance with whether said received data signal is advanced or retarded relative to said output clock signal.